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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg

Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Docket No.: 303.522US1
Filed: August 25, 1999
Examiner: Richard Booth

Serial No.: 09/382,442
Due Date: April 18, 2005
Group Art Unit: 2812

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Name

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

PATENT

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IN A MEMORY CIRCUIT	)	

APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

BOX Appeal Brief
Commissioner for Patents
Washington, D.C. 20231

Sir:

This Supplemental Appeal Brief is filed in Response to the Notice of Non-Compliant Appeal Brief mailed March 16, 2005 and presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on January 14, 2004, from the Final Rejection of claims 1-2 and 4-14, 26-32, and 35-39 of the above-identified Application, as set forth in the Final Office Action dated October 14, 2003.

The original Appeal Brief was accompanied by the requisite fee set forth in 37 C.F.R. § 117(c). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims 1-2 and 4-14, 26-32 and 35-39.

APPELLANTS' SUPPLEMENTAL BRIEF ON APPEAL

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1. Real Party in Interest

The real party in interest is Micron Technology, Inc.

2. Related Appeals and Interferences

There are no related appeals or interferences.

3. Status of the Claims

On January 14, 2004, appellant appealed from the final rejections of claims 1-2 and 4-14, contained in the office action dated October 14, 2003. The claims on appeal are set forth in Appendix A.

4. Status of Amendments

No amendment has been filed subsequent to the February 11, 2003 Restriction Requirement and the Office Action. The claims are as last amended in the paper filed by appellant on March 11, 2003, in response to the Restriction Requirement.

5. Summary of the Invention

Appellant's invention relates to a method for reducing single bit data loss in a FLASH memory circuit having a programming operation and an erase operation. The method includes providing a semiconductor layer having a surface and heating the semiconductor layer in an atmosphere comprising a hydrogen isotope, wherein the hydrogen isotope is incorporated into the layer. The method also includes fabricating a memory circuit having a programming operation and an erase operation comprising single bit data using the semiconductor layer, wherein the hydrogen isotope is incorporated. The fabricating includes fabricating a gate region in the semiconductor layer, treating a portion of the surface to form a thin layer of insulator film adjacent to the gate region and under the gate region; and heating the thin layer in an atmosphere comprising hydrogen isotope, wherein single bit data loss is reduced and wherein random single bit data loss is prevented in both the programming operation and the erase operation.

6. Issues Presented for Review

Claims 1-14, 26-32 and 35-39 are pending in the case. Claims 3, 26-32, and 35-39 are withdrawn. Claims 1-2, and 4-14 remain in the application and are the subject of this appeal.

A final office action mailed October 14, 2003, rejected claims 1-2, 4-5 and 7-10 under 35 U.S.C. 103(a) as being unpatentable over Nakanishi, U.S. Patent 5,145,797 in view of Lisenker et al., WO 94/19829 and further in view of what the Examiner called, "Admitted prior art." The "Admitted Prior Art" referred to by the Examiner was initially described in an office action of June 20, 2001. In this office action, the Examiner stated, "Admitted prior art shows the invention as claimed including the fact that EPROMs are subject to problems related to hot carrier degradation (see specification, page 2, line 28—page 5, line 6). The admitted prior art in the specification fails to disclose using deuterium to cure the hot electron degradation affect."

In the final office action of October 14, 2003, the Examiner rejected claim 6 under 103(a) as being unpatentable over Nakanishi, U.S. Patent 5,145,797 in view of Lisenker et al., WO 94/19829 and further in view of "Admitted prior art" as applied to claims 1-2, 4-5, and 7-10 above, and further in view of Nakajima et al., U.S. Patent 5,397,724.

In the final office action of October 14, 2003, the Examiner also rejected claims 11-14 under 103(a) over Nakanishi, U.S. Patent 5,145,797 in view of Lisenker et al., WO 94/19829 and further in view of Admitted prior art as applied to claims 1-2, 4-5, and 7-10 above and further in view of Sheu, U.S. Patent 4,840,917.

A tabular summary of the basis of 103 rejection for each claim is as follows:

Claim No.	References Cited in Final Office Action
1	Nakanishi, Lisenker, "Admitted Prior Art"
2	Nakanishi, Lisenker, "Admitted Prior Art"
4	Nakanishi, Lisenker, "Admitted Prior Art"
5	Nakanishi, Lisenker, "Admitted Prior Art"
6	Nakanishi, Lisenker, "Admitted Prior Art," Nakajima
7	Nakanishi, Lisenker, "Admitted Prior Art"
8	Nakanishi, Lisenker, "Admitted Prior Art"
9	Nakanishi, Lisenker, "Admitted Prior Art"
10	Nakanishi, Lisenker, "Admitted Prior Art"

11	Nakanishi, Lisenker, "Admitted Prior Art," Sheu
12	Nakanishi, Lisenker, "Admitted Prior Art," Sheu
13	Nakanishi, Lisenker, "Admitted Prior Art," Sheu
14	Nakanishi, Lisenker, "Admitted Prior Art," Sheu

7. Grouping of Claims

Appellant is appealing the final rejection of claims 1-14, 26-32, and 35-39 under 35 U.S.C. 103(a) as set forth in the final office action. Appellant is grouping claims in the following manner:

Group I: 1-2, 4-5, 7-10

Group II: 6

Group III: 11-14

Claims 26-32 and 35-39 have been withdrawn.

8. Argument

Group I

Claims 1-2, 4-5, and 7-10, Group I, were rejected under 35 USC Sec. 103(a) as being unpatentable over Nakanishi (U.S. 5,145,797) in view of Lisenker et al. (WO 94/19829) and further in view of what the Examiner described as "admitted prior art," as described above. The Examiner maintained the rejection in a statement filed in conjunction with an Advisory Action, mailed September 22, 2003. In response to the Appellant's position that the references did not suggest combination, the Examiner stated that "the rejection is proper."

Claim 1 describes a method for reducing random single bit data loss in a FLASH memory circuit having a programming operation and an erase operation. The method includes providing a semiconductor layer having a surface; heating the layer in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer; and fabricating a memory circuit having a programming operation and an erase operation, comprising single bit data using the semiconductor layer, the fabricating comprising fabricating a gate region in the layer; treating a portion of the surface to form a thin layer of insulator film adjacent to the gate region and under the gate region; and heating the thin layer in an atmosphere comprising Hydrogen isotope, wherein single bit data loss is reduced and wherein random single bit data loss is prevented in both the programming operation and the erase operation.

Claims 2, 4, 5 and 7-10 describe method steps and features that require deuterium treatment.

The Nakanishi patent has been cited by the Examiner in combination with the Lisenker application to argue that claim 1 is obvious. The Nakanishi patent describes a method that is directed to forming a flash-type EEPROM structure that includes a P-type silicon substrate that is thermally oxidized to form a gate insulating film. A polysilicon film is deposited on the P-type silicon substrate with a phosphorus impurity diffused into it to form a layer. This layer is then thermally oxidized to form an interpolysilicon-layer insulating film. A second layer polysilicon film, used for a control gate electrode is deposited on the interpolysilicon-layer insulating film. The layers are then etched. After etching, the sidewall of the floating gate electrode is thermally oxidized in dry oxygen at 900 degrees C. Arsenic is then implanted to form a source region and a drain region.

The Nakanishi patent has no reference to a use of hydrogen isotopes. The Nakanishi patent's reference related to fabricating the floating gate electrode occurs when the Nakanishi patent refers to the floating gate electrode as being "thermally oxidized in **dry oxygen** atmosphere at 900 degrees Centigrade to form an ion implantation-induced damage protection film 7 (a mask oxide film)." Col. 2, lines 49-51. The dry oxygen atmosphere described does not include hydrogen or deuterium and, Appellant asserts, teaches away from what is claimed in claims 1-2, 4-5 and 7-10 because dry oxygen excludes a use of hydrogen or hydrogen-containing material such as water. Thus, Appellant asserts that there is no motivation to combine the method of Nakanishi, which describes floating gate fabrication in an atmosphere free of hydrogen with the Lisenker patent application which describes a method used in wet oxygen treatment. See page 5, lines 9-11. To the contrary, the Nakanishi patent teaches a use of a dry oxygen atmosphere for treating its floating gate electrode.

Page 8 of the Lisenker application describes the Lisenker method as usable in processes that employ hydrogen. The Nakanishi patent, on the other hand, describes a process that does not employ hydrogen. The only thermal step that is described with some detail in Nakanishi refers to a "dry oxygen atmosphere." Thus, Nakanishi teaches away from the claimed invention which requires hydrogen. Furthermore, because Nakanishi describes an oxidation process that does not include hydrogen, and Lisenker describes a process that does include hydrogen, the references are directed to antithetical processes. Appellant asserts that the patents cannot then be properly combined.

The Lisenker reference does not stand alone in rendering the claimed invention obvious because the Lisenker reference does not refer a use of deuterium for reducing random single bit data loss in a FLASH memory cell. This omission, acknowledged by the Examiner, is significant because FLASH memory includes a programming operation and an erase operation. Both the programming operation and the erase operation must operate in a satisfactory manner for the FLASH memory to perform acceptably. None of the MOSFET devices, TFT's, polyresistors or polyemitter bipolars described in the Lisenker reference operate with this two step programming operation and erase operation. Thus, there is no suggestion in the Lisenker reference cited by the Examiner for concluding that deuterium substitution would work to reduce random single bit data loss in a memory cell.

Furthermore, the observations described in the Lisenker et al. patent suggest that deuterium treatment would not be effective in an erase operation because deuterium does not have the same removal properties as hydrogen. Thus, there is no suggestion that single bit data loss is reduced by deuterium because the Lisenker reference provides no description of how deuterium impacts erasing operations.

The Examiner stated in the Advisory Action of December 14, 2001, that the Lisenker reference does discuss FLASH memory and the effectiveness of deuterium in erasing operations. However, the Examiner declined to cite a passage in the Lisenker reference where this discussion occurred.

Appellant therefore asserts that the Lisenker patent application provides no support for rendering claim 1 obvious, wherein random single bit data loss in a FLASH memory circuit having a programming operation and an erase operation is reduced by deuterium treatment in and under the gate region, because Lisenker provides no support for the proposition that deuterium is usable in a process that includes erasing operations. Nakanishi describes a FLASH memory circuit fabrication but the fabrication proximal the gate includes a dry oxidation, free of hydrogen. This type of oxidation treatment is contrary to what is required for deuterium treatment. Thus, Appellant asserts that the combination of Lisenker and Nakanishi do not render the invention described herein obvious.

Group II

Claim 6 describe the method of claim 1 "and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature."

For reasons discussed above, the Lisenker reference and the Nakanishi reference and the so called "admitted prior art" do not render claim 1 obvious. Claim 6 depends from claim 1 and further specifies that the semiconductor layer be exposed to "atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature." Neither the Lisenker reference nor the Nakanishi reference describes exposing the semiconductor layer of a FLASH memory device to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature in order to reduce single bit data loss.

The additional reference cited by the Examiner, the Nakajima reference, does not remedy this issue either. The Nakajima reference refers to wet oxidation but in column 6, lines 43-50, the reference describes a heating step that improved data retention. The heating step description does not include hydrogen or deuterium. Instead, the Nakajima et al. reference describes an insulating film doped with phosphorus. Thus, the Nakajima reference does not describe a step of exposing the semiconductor layer to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature as is claimed.

Group III

The claims in Group III are directed to the method of claim 1 and further comprising forming a field oxide in the semiconductor layer. The claims are also directed to the method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound. The Lisenker, Nakanishi references and "admitted prior art" do not describe a method for reducing single bit data loss in a FLASH memory cell by forming a field oxide in a semiconductor layer of a FLASH memory cell and annealing the field oxide in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

The Sheu patent, cited by the Examiner, describes methods for introducing atomic hydrogen into MNOS capacitors to reduce the Si/SiO(2) interface state density. The Sheu reference does not discuss deuterium and is not directed specifically to FLASH memory with an erase feature. Sheu describes sintering aluminum with hydrogen in construction of an unpatterned aluminum layer. The Sheu patent provides no support for the proposition that deuterium is usable in a process that includes erasing operations. The Sheu patent did not even recognize that deuterium does not have the same removal properties as hydrogen. Thus, Appellant asserts that the combination of Nakanishi and Sheu does not then render the present invention obvious.

The Examiner relies upon the In re Keller case, 642 F.2d 413 (Ct. Customs & Pat. Appeals) to support combining the Lisenker Nakanishi patents and Sheu references. The Keller case concerned a mechanical/electrical device, a pacemaker, and not a chemical process as is claimed herein. All of the devices in the combined references discussed in the In re Keller case were pacemakers. The claim in contention in the Keller case included means plus function

language. The art cited by the Examiner in the Keller case described pacemakers with different types of timers. The Court in Keller determined that the pacemaker system was a "plug and play" system and that one skilled in the art could see that different types of timers—digital as opposed to analog, were equivalent options, in terms of means plus function, in a substitution array.

The claims in the present invention are chemical and material science in nature and do not include means plus function language. Appellant asserts that there is considerably less predictability in chemical systems and material science systems generally than in mechanical systems, such as the system described in Keller. Appellant also asserts that the aluminum sintering of the Sheu patent, dry oxygen surface treatment described in Nakashimi, and phosphorus doping treatment of Nakajima are not interchangeable elements in a "plug and play" system in FLASH memory design. Therefore, Keller is not appropriate support for the Examiner's position. Furthermore, only one of the references, Lisenker, describes a use of deuterium. The other references describe uses of water or water-free processes. Appellant asserts that the processes described in the references relied upon by the Examiner are not equivalent in function to the deuterium treatment claimed and that the processes are not used interchangeably the same way that the mechanical elements were interchanged in the Keller case.

9. Summary

For the foregoing reasons, it is submitted that the examiner's rejections of claims 1-2, 4-5, 6, 7-10, and 11-14 were erroneous. Reversal of those holdings is respectfully requested. Should the Board be of the opinion that a rejected claim may be allowable in amended form, an explicit statement to that effect is also respectfully requested.

Respectfully submitted,

By their Representatives,

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Date 18 Apr 05 By _____
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Tina Kahwl
Name

_____
Signature

APPENDIX I

The Claims on Appeal

1. (Rejected) A method for reducing random single bit data loss in a FLASH memory circuit having a programming operation and an erase operation, comprising:

providing a semiconductor layer having a surface;

heating the layer in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer; and

fabricating a memory circuit having a programming operation and an erase operation, comprising single bit data using the semiconductor layer, the fabricating comprising fabricating a gate region in the layer; treating a portion of the surface to form a thin layer of insulator film adjacent to the gate region and under the gate region; and heating the thin layer in an atmosphere comprising Hydrogen isotope, wherein single bit data loss is reduced and wherein random single bit data loss is prevented in both the programming operation and the erase operation.

2. (Rejected) The method of claim 1 and further comprising forming a film on the semiconductor layer that comprises the Hydrogen isotope.

3. (Cancelled)

4. (Rejected) The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that oxidizes the semiconductor layer.

5. (Rejected) The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that anneals the semiconductor layer.

6. (Rejected) The method of claim 1 and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.

7. (Rejected) The method of claim 1 and further comprising fabricating a second gate region within the memory circuit.

8. (Rejected) The method of claim 7 and further comprising forming a film comprising Hydrogen isotope adjacent to the gate region of the memory circuit in order to reduce single bit data loss.

9. (Rejected) The method of claim 7 and further comprising forming a film comprising Hydrogen isotope within the gate region of the memory circuit in order to reduce single bit data loss.

10. (Rejected) The method of claim 1 and further comprising passivating the semiconductor layer in an atmosphere comprising Hydrogen isotope.

11. (Rejected) The method of claim 1 and further comprising forming a field oxide in the semiconductor layer.

12. (Rejected) The method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

13. (Rejected) The method of claim 11 and further comprising annealing at a temperature that is at least about 800 degrees Centigrade.

14. (Rejected) The method of claim 11 and further comprising oxidizing the annealed field oxide layer in an atmosphere that comprises Hydrogen isotope.

15-25. (Cancelled)

26. (Withdrawn) A method of forming a non-volatile electrically alterable semiconductor FLASH memory cell having a programming operation and an erase operation, with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

heating the silicon substrate in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

heating the silicon substrate with the field oxide region and channel region in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer;

growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell having a programming operation and an erase operation, comprising single bit data loss in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss, wherein random single bit data loss is prevented in both the programming operation and the error operation.

27. (Withdrawn) The method of claim 26 and further including nitridizing the field oxide region by annealing in an atmosphere comprising Hydrogen isotope or a compound that comprises Hydrogen isotope.

28. (Withdrawn) The method of claim 26 and further comprising nitridizing at a temperature that is greater than or equal to about 800 degrees Centigrade.

29. (Withdrawn) The method of claim 26 and further including oxidizing the nitridized field layer in an atmosphere that comprises Hydrogen isotope.

30. (Withdrawn) The method of claim 26 and further comprising introducing the Hydrogen isotope by thermal oxidation.

31. (Withdrawn) The method of claim 26 and further comprising introducing the Hydrogen isotope by pyrolytic diffusion of Hydrogen isotope into the memory cell.

32. (Withdrawn) The method of claim 26 and further comprising introducing the Hydrogen isotope by RF sputter deposition.

33-34. (Cancelled)

35. (Withdrawn) A method for treating a non-volatile, electrically alterable semiconductor memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell comprising single bit data; and

exposing the memory cell to an atmosphere that comprises Hydrogen isotope by sputter deposition or pyrolytic diffusion, thereby reducing single bit data loss.

36. (Withdrawn) The method of claim 35 and further including heating the atmosphere.

37. (Withdrawn) A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell having a programming operation and an erase operation, with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate and providing a memory cell, having a programming operation and an erase operation, the memory cell comprising single bit data;

defining source and drain regions in the silicon substrate and exposing the source and drain regions to an environment comprising Hydrogen isotope; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss in the programming operation and the erase operation in the memory cell.

38. (Withdrawn) The method of claim 37 and further comprising heating the atmosphere that comprises Hydrogen isotope.

39. (Withdrawn) The method of claim 37 and further comprising defining the source and drain regions by targeted Hydrogen isotope implantation.